

Prototype of Readout Electronics for the ED in LHAASO KM2A *

LIU Xiang()^{1,2,3,1)} CHANG Jing-Fan()^{1,2,3,2)} WANG Zheng()^{1,2,3} FAN Lei()^{1,2,3}

¹ State Key Laboratory of Particle Detection and Electronics, Chinese Academy of Sciences, Beijing 100049, China

² Institute of High Energy Physics, Chinese Academy of Sciences, Beijing 100049, China

³ University of Chinese Academy of Sciences, Beijing 100049, China

Abstract: The KM2A (one kilometer square extensive air shower array) is the largest detector array in the LHAASO (Large High Altitude Air Shower Observatory) project. The KM2A consists of 5635 EDs (Electromagnetic particle Detectors) and 1221 MDs (Muon Detectors). The EDs are distributed and exposed in the wild. Two channels, Anode and Dynode, are employed for the PMT (photomultiplier tube) signal readout. The readout electronics proposed in this paper aims at the accurate charge and arrival time measurement of the PMT signals, which cover a large amplitude range from 20 P.E (photoelectrons) to 2×10^5 P.E. By using the Trigger-less architecture, we digitize signals close to the PMTs. All digitized data is transmitted to DAQ (Data Acquisition) via the simplified WR (White Rabbit) protocol. Compared with traditional high energy experiments, high-precision of time measurement in such a large area and suppression of temperature effects in the wild become the key techniques. Experiments show that the design has fulfilled the requirements in this project.

Key words: LHAASO, ED, readout electronics, WR

PACS: 84.30.-r

1 Introduction

The LHAASO (Large High Altitude Air Shower Observatory) [1] is a multi-objective project aiming at searching the origin of high energy galactic cosmic rays with a 1.2 km^2 complicated ground detector array. The KM2A (one kilometer square extensive air shower array), designed for the measurement of the number density and arrival time of shower particles, contains 5635 EDs (Electromagnetic particle Detectors) and 1221 MDs (Muon Detectors) [2]. All EDs are evenly distributed in the one square kilometer wild area.

Signals from PMTs vary in a large dynamic range from 20 P.E (photoelectrons) (single particle) to 2×10^5 P.E (10^4 particles) [3], because of the large primary energy of the cosmic rays (10 TeV-100 TeV) and the dif-

ferent distances between detectors and shower cores. To cover the whole dynamic energy range and guarantee the accurate case reconstruction, precise charge and time measurements should be achieved in readout electronics. In this broad area, we need to read out 5635 PMTs in total. As for charge measurement, a resolution of 25% at single particle is required for each channel. And the RMS (root mean square) of time measurement is demanded to be better than 1 ns (nanosecond) while the bin size is better than 2 ns, which means that the high quality of clock synchronization and distribution in a large scale is required. Furthermore, the performance stability become a great challenge because the electronics will be running in the wild and the temperature can vary from -5°C to $+50^\circ\text{C}$ in the high altitude observatory. To sum up, the requirement for electronics is list in Table 1.

Table 1. Requirement of the ED readout electronics

Item	Requirement
Dynamic range of charge measurement	1-10000 particles
Resolution of charge measurement	25% @ 1 particle; 5% @ 10000 particle
Bin size of time measurement	< 2 ns
Resolution of time measurement	< 1 ns
Case rate when threshold is set 0.125 particle	2 KHz
Temperature range	$-5^\circ\text{C} - +50^\circ\text{C}$

Received 14 March 2009

* Supported by National Natural Science Foundation of China (11375210) and the Knowledge Innovation Fund of IHEP, Beijing

1) E-mail: liuxiang@ihep.ac.cn

2) E-mail: changjif@ihep.ac.cn

©2013 Chinese Physical Society and the Institute of High Energy Physics of the Chinese Academy of Sciences and the Institute of Modern Physics of the Chinese Academy of Sciences and IOP Publishing Ltd

In the view of the distributed architecture of detectors, the traditional electronics system based on VME case is significantly unpractical. Instead, we adopt a trigger-less, separate, front-end architecture, in which we place electronics nearby the PMT to achieve the purpose of maintaining signal characteristics and reducing the number of signal cables. Digitized data, commands and clocks are transferred via a single optical fiber.

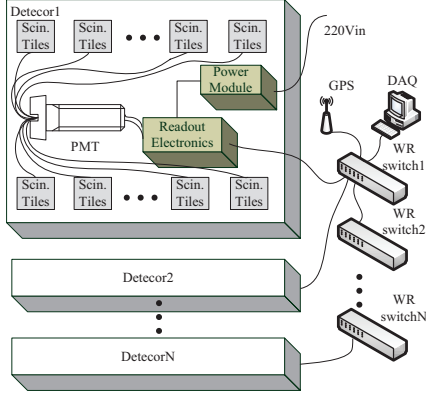


Fig. 1. Architecture of EDs

Fig. 1 shows the structure of EDs. The readout electronics, power module are placed in the same shell with tiles and PMT. The 220V AC (alternating current) power is modulated to 6V DC(direct current) supply for the electronics and settable high-voltage supply for PMT. Each ED consists of 16 scintillator tiles which are readout by wavelength-shifting fibers bundled and fixed by a 25mm PMT[4]. Signals from PMT are transmitted to the electronics via two independent 50cm cables.

The local clocks of ED readout electronics are synchronized by a global high precision 125MHz clock, which is created and distributed based on the simplified WR(White Rabbit) protocol[5]. This protocol is proposed by CERN and simplified by Tsinghua University, and developed to provide a sub-nanosecond accuracy and picosecond precision of synchronization. The synchronized clock can be distributed to thousands of WR nodes within 10km, while the timing and data link are combined over the same physical media. Experiments show that clocks of two WR nodes can be synchronized with 100ps(picoseconds) accuracy and 20ps precision[6][7]. According to WR protocol, a CUTE-WR(compact universal timing endpoint based on the WR) is required in the timing synchronization. In this system, the CUTE-WR hardware is fused into the readout electronics. Function of CUTE-WR is recovering the TAI (international atomic time), PPS(pulse per second) and synchronized 125MHz clock. Besides, a standard network interface is supplied for data transmission.

Compared with the architecture of global trigger in traditional experiments such as BESIII[8] and

LAWCA[9], ED readout electronics needs no trigger electronics. Data discriminated by the threshold is transmitted to DAQ(Data Acquisition) and the kernel trigger processing is also completed in DAQ. The TUTE-WR contains a programmable core named WRPC(WR PTP core)[10], which can serve as an Ethernet MAC in FPGA. In order to improve the reliability of data transmission, an implementation of TCP/IP protocol based on FPGA, cooperating with WRPC has been developed to forward and receive data packages between readout electronics and DAQ. The results tell that the maximum throughput of 320Mbits per second can be achieved in this realization[11], that is sufficient for the ED readout system due to the highest case rate of PMT is 2KHz when the threshold is set to 1/8 particle.

2 The ED Readout Electronics

The architecture of ED readout electronics is designed and measured as shown in Fig. 2. Signals from Anode and Dynode are digitized by a two-channels, 65MHz ADC(Analog to Digital Converter) after handled by the amplification and shaping circuit. Then, the digitized signals is sent to FPGA for digital peaking. Signals from Anode are also amplified and compared with the threshold to trigger time measurement. This trigger is delivered to FPGA and then digitized by a TDC (time to digital converter) integrated in the FPGA.

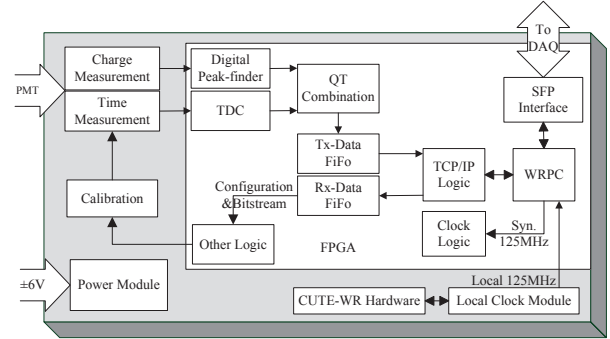


Fig. 2. Block diagram of ED readout electronics

Digitized charge and time information is combined and buffered in Tx-FIFO. The TCP/IP module read and send the data in Tx-FIFO in each millisecond. Configuration data, control commands and the bitstream files is received and buffered in the Rx-FIFO. The WRPC adjust local 125 MHz clock provided by onboard crystal oscillator to a synchronized referent clock, which can be regulated to 62.5MHz clock for system process and 250MHz clock for TDC module.

2.1 Charge Digitizing Module Design

To achieve the large scope as mentioned and get a enough overlap, two electronics channels and two PMT

readout channels are employed. The Anode electronics channel covers a range of $1 \sim 200$ particles while the Dynode channel covers a range of $100 \sim 10^4$ particles. And the ratio of gain between two channel is designed 2 times.

The charge digitizing circuit is shown in Fig. 3. To achieve the high precision of charge measurement and better temperature performance, this circuit abandon the input buffer compared with the readout electronics for WCDA(water Cherenkov detector array)[12] in LHAASO. Simulation and experiments shows that the offset voltage of the buffer amplifier is obviously amplified by integral circuit. So, a little swing of this offset voltage can literally deteriorate the SNR(signal-noise ratio) of the charge measurement. Whats more, the amplified offset voltage is tested to vary evidently with the temperature shift.

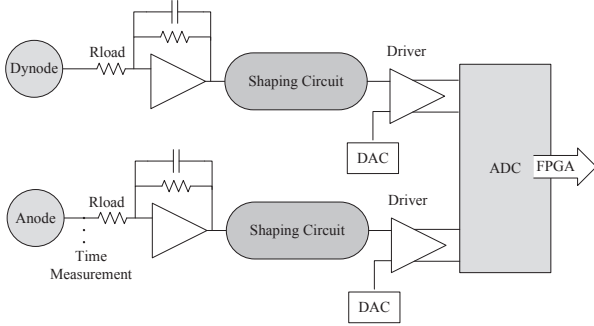


Fig. 3. Design of charge digitizing module

In this design, current signals from PMTs are directly sent to integral and shaping circuit. The peak value digitized by ADC and sought in FPGA can quantitatively represent the charge of input signal. The gain resistor in the integral circuit is devised to be 500 Ω to serve as an input load resistor. Voltage signals for time measurement is also sampled at the gain resistor of anode channel.

To reduce the effect of temperature, the DC performance of the amplifiers becomes significant. Amplifiers with lower input offset voltage drift are selected in this design. By the way, the inverting input of the ADC differential driver is supposed to source from low drift referent DAC(digital to analog converter) instead of mechanical potentiometer.

2.2 Time Digitizing Module design

The technology of Multi-phase TDC[13] based on FPGA is applied to measure arrival time of Anode signal, as illustrated in Fig. 4. Voltage sampled from Anode is magnified 20 times by two steps. We assign the gain of the first step to be +2 for the input high-impedance state, therefore, the input impedance of Anode keeps 500 Ω .

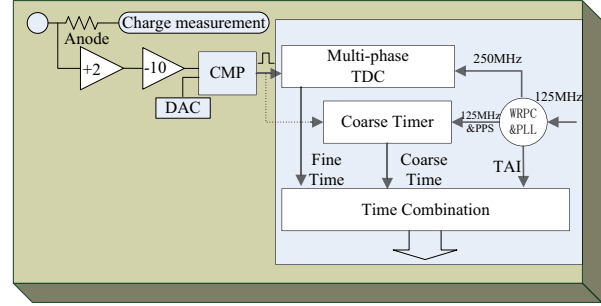


Fig. 4. Design of time digitizing module

In consideration of the waveform of the PMT signal, the voltage sampled from the 500 Ω resistor is about 8mV when the Anode input signal equal single particle. A 2.5V full-scale, 12bits DAC is employed as a threshold generator. Since the step of DAC is 0.61 mV, threshold of time measurement can accurately be set to 1/8 particle.

The time digitizing module integrated in the FPGA is triggered by the rising edge from comparator. All clocks related in this section originate from the synchronized 125MHz. The coarse time counter is driven by a 125 MHz clock and reset by the PPS signal, so the dynamic range of time measurement is 1s. Four 250MHz phase-shifted clocks drive the fine time measurement, the bin size of the TDC is 1ns in this way. Finally, the TAI time from WRPC, coarse time from coarse counter and fine time from multi-phase circuits constitute the arrival time of signals.

The lower input offset voltage drifts of amplifiers and DAC contribute to the better temperature performance. On the other hand, the routing length of trigger signals from comparator to the first flip-flop in the FPGA should be controlled because the routing delay is also proved to drift with temperature changing.

3 Performances of the ED Readout Electronics

3.1 Charge Digitizing Module evaluation

To evaluate the charge measurement in laboratory, we set the frequency of generated signal to the maximum event-ratio 2kHz. And the peak value of anode signals is adjusted from 8mV to 1600mV to cover the full range. Correspondingly, the dynode signals is adjusted from 4mV to 700mV.

Resolution of the minimum charge measurement is shown in Fig. 5, where Mean and RMS are the mean value and standard deviation of signals. According to the left figure, the resolution of Dynode charge measurement is calculated to 2.19%, and a 4.88% precision of anode can be deducted from right figure.

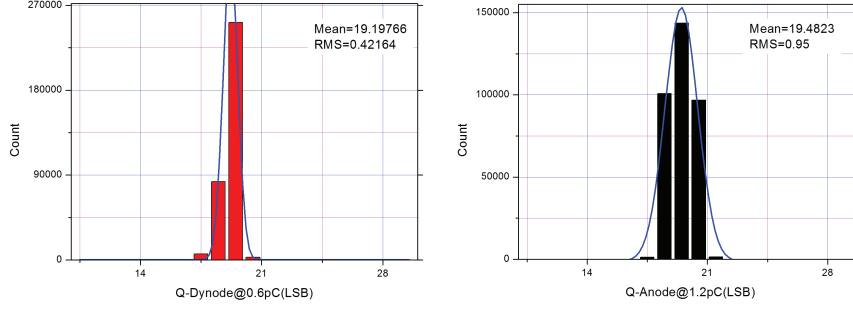


Fig. 5. Precision of the minimum signals

Table 2. Contrast result of precision

	<i>Anode</i>	<i>Anode(experimental)</i>	<i>Dynode</i>	<i>Dynode(experimental)</i>
<i>Mean(LSB)</i>	19.48	22.57	19.20	24.07
<i>RMS(LSB)</i>	0.95	3.01	0.42	4.17
<i>Precision</i>	4.88%	13.33%	2.19%	17.32%

To verify the influences of input buffer on the precision as described, we similarly test the performance of experimental board which is equipped with input buffers both in dynode and anode channel. Table 2 tells the con-

trast result. Although the precision can also fulfill the requirement of 25%, the input buffers clearly worsen the performances of charge measurement.

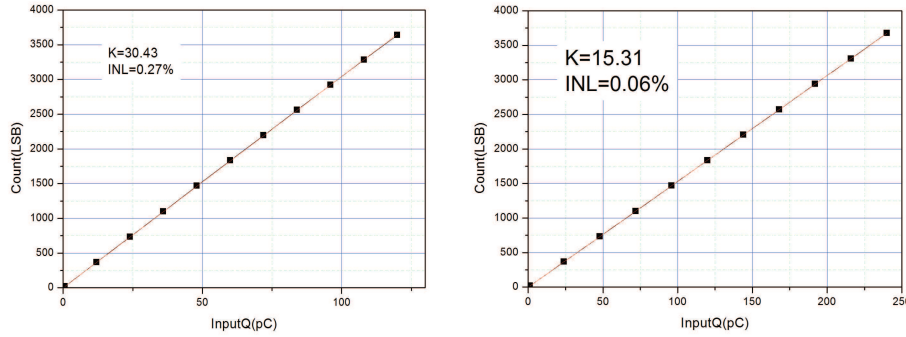


Fig. 6. INL of charge digitizing module

The INL(integral non-linearity) of charge digitizing module is tested as shown in Fig. 6. The K means the gain of ADC readout to input charge. The proportion between dynode and anode is proved to be 1.98.

3.2 Time Digitizing Module evaluation

A statistical code density test based on a source of random hits[13] is used to evaluate the INL of time digitizing module. Since the coarse counter is driven by 125MHz clock, the fine time is divided to 8 bins. The maximum INL achieved 0.03LSB as shown in Fig. 7.

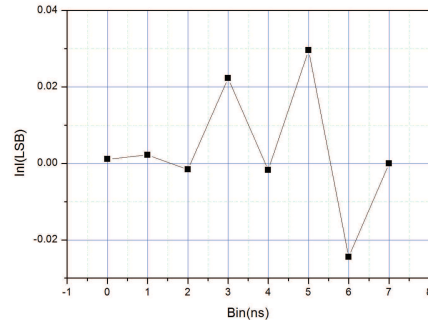


Fig. 7. INL of time digitizing module

In the precision test, threshold is set at 1/8 particle. Fig. 8 shows the precision in different situations: the minimum input signals and the maximum input signals. Result indicates that the accuracy maintains better than 0.5ns no matter with the peak value of signals in laboratory.

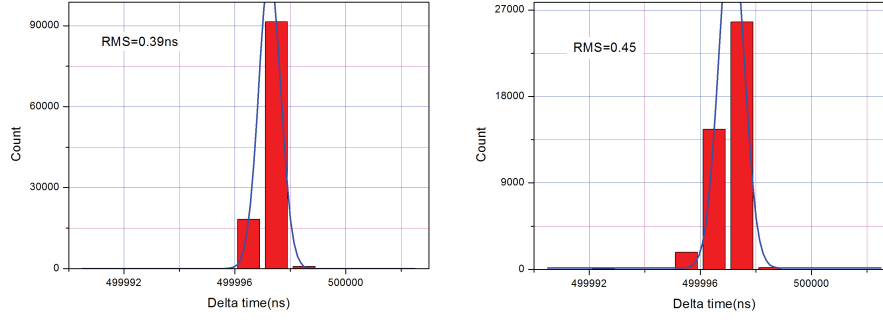


Fig. 8. Precision of time digitizing module in laboratory

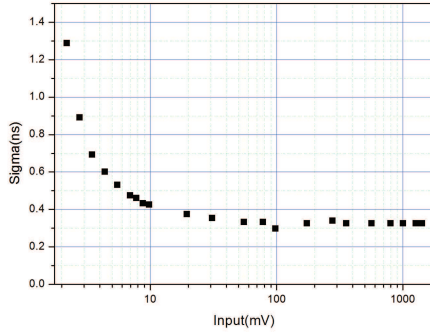


Fig. 9. Precision of time digitizing module with PMT

However, experiment associating with PMTs shows that the precision gets worse when the input signal get smaller, as shown in Fig. 9. The time-walking and noise of input signals contribute to the phenomenon that the accuracy is worse than 0.5 ns when the peak value of signals get lower than 0.5 particle. In any case, this result has reached the target.

3.3 Temperature performance

As one of the key performances, the temperature effect is taken into special consideration in the system design. To assess this performance, we propose an experiment as shown in Fig. 9. In this experiment, two synchronized readout boards are employed to test exactly same signals generated by the same generator. One of the two boards is placed under the normal condition to serve as a reference, while the other one is put in a thermostat, in which the temperature is programmed to varying from -10°C to $+60^{\circ}\text{C}$.

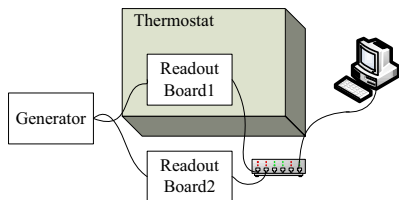


Fig. 10. Temperature performance experiment

Then, the charge and time information of two boards in different situations reflect the temperature performance. The temperature of charge measurement is shown in fig. 11. The Anode charge measurement presents a same trend with Dynode when temperature changes. The ADC output data has a tiny change in the whole temperature range while the input signals keep fixed. The ADC output varies less than 0.8% in 70°C , this characteristic has achieved the target because the PMT temperature coefficient is proved to be 0.2% in 1°C .

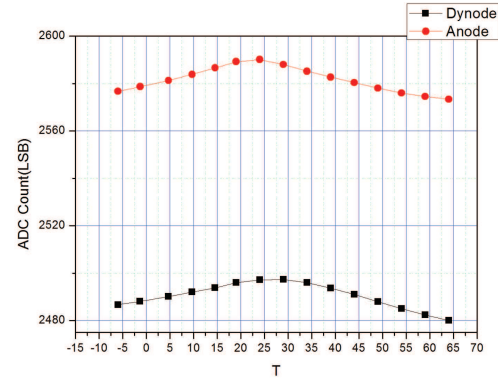


Fig. 11. Temperature performance of charge measurement

As presented in fig. 12, the arrival time tested by two boards keeps a 6 ns delay because the different length of cables. This delay changes less than 150 ps in 70°C , which means that no correction is necessary in DAQ.

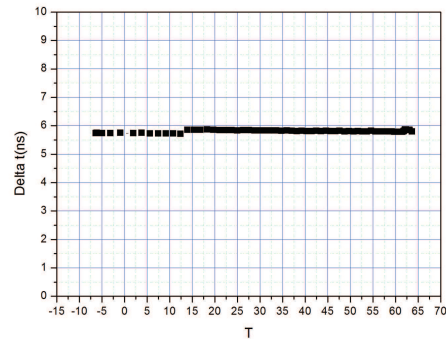


Fig. 12. Temperature performance of time measurement

4 Conclusion

In this paper we propose a readout electronics system used for EDs in LHAASO KM2A. Each performances have meet the requirements and every index is proved to be stable in the large temperature range. With the technology adopted in this paper, readout electronics system

can be designed for the high energy experiments built in the large, harsh environment.

5 Footnotes

We thank PAN Weibin and LI Hongming of Tsinghua University and LIU Jia of IHEP for their help.

References

- 1 CAO ZHEN et al. A future project at tibet: the large altitude air shaower observatory(LHAASO),Chin.,Phys.C,2010,34(2):249-252.
- 2 HE Hui-hai et al. LHAASO Project: detector desian and prototype, Proceedings of hte 31 st ICRC,2009.
- 3 Lv Hong-kui. Extension of photomultiplier tube dynamic range for the LHAASO-KM2A Eletromaganetic particle detectors,Nuclear Insruments and Methods in Physics Research A,781(2015):34-38.
- 4 ZHAO jing. Design and performances of electromagnetic particle detector for LHAASO-KM2A.,Chin.,Phys.C,2014,38(3)036002.
- 5 J.Serrano et al.The White Rabbit Project, Proceedings of ICALEPCS TUC004,Kove,Japan,2009
- 6 Pan Wei-bin et al.High resolution distrubuted time-to-digital converter(TDC) in a White Rabbit network,Nuclear Insru-
ments and Methods in Physics Research A,738(2014):13-19.
- 7 G.Gong et al. Sub-nanosecond timing system design and development for LHAASO project, Proceedings of ICALEPCS,Grenoble,France,2011
- 8 LIU Zhen-an et al.Trigger System of BESIII,Proceedings of the 15th Real-Time Conference, Ed. Hao B. Chaos,2007
- 9 YAO Lin.A prototype of trigger electronics for LAWCA experiment,Chin.,Phys.C,2013,34(12)126101
- 10 White Rabbit PTP core (WRPC),(<http://www.ohwr.org/projects/wr-cores/wiki>)
- 11 ZHAO Yi-ran. FPGA implementation of TCP/IP Protocol,master of science thesis,University of Chinese Academy of Sciences, 2015.
- 12 ZHAO Lei.Proposal of the readout eletronics for hte WCDA in the LHAASO experiment, Singapore,Chin.,Phys.C,2014,38(1)016101
- 13 M.Fries et al"High-precision TDC in an FPGA using a 192 MHz quadrature clock,IEEE Nuclear Science Syosium Conference Record.2002,1:580-584